General Descirption

The OC3001 is a single Phase 12V MOSFET gate drivers optimized to drive the gates of both high−side and low−side power MOSFETs in a synchronous buck converter. The high−side and low−side driver is capable of driving a 3nF load with a 25ns propagation delay and a 30ns transition time.

With a wide operating voltage range, high or low side MOSFET gate drive voltage can be optimized for the best efficiency. The internal adaptive non-overlap circuit further reduces the switching losses by preventing simultaneous conduction of both MOSFETs.

The floating top driver design can accommodate BST voltages as high as 40V, with transient voltages as high as 48V. Both gate outputs can be driven low by applying a low logic level to the OD pin. An UVLO function ensures that both driver outputs are low when the supply voltage is low, and a Thermal Shutdown function provides the IC with over-temperature protection.

OC3001 is available in SOP8 and DFN8 package.

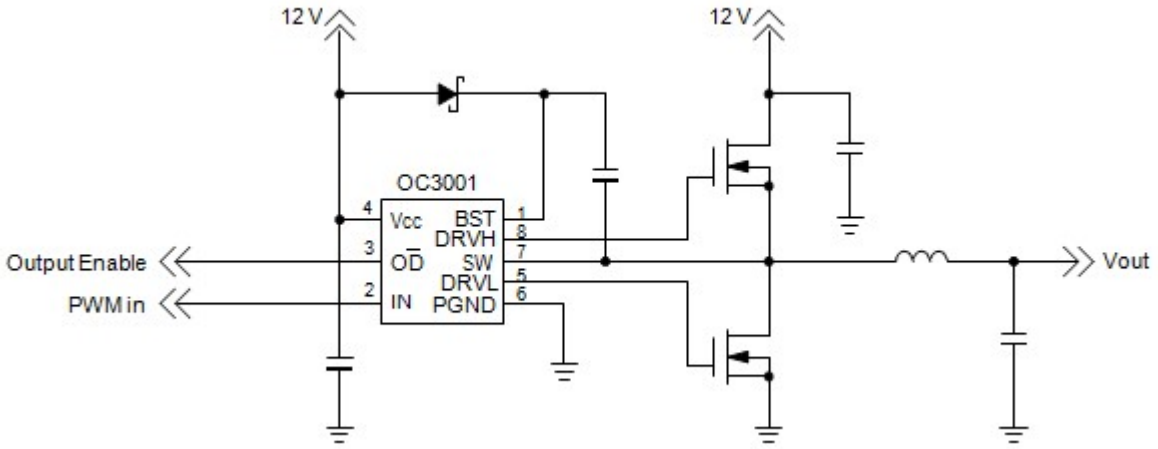
Features

- All−In−One Synchronous Buck Driver
- Bootstrapped High−Side Drive
- One PWM Signal Generates Both Drives
- Anti-cross Conduction Protection Circuit
- These are Pb−Free Devices

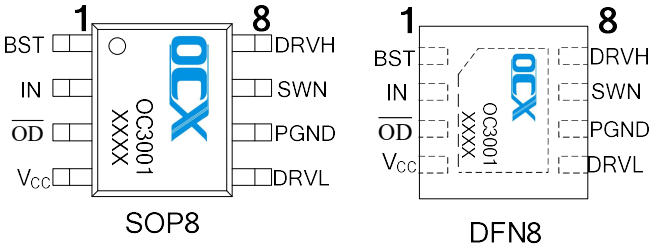
Applications

- Multiphase Desktop CPU Supplies
- Single−Supply Synchronous Buck Converters
- e-cigarette
- wireless charger

Typical applicaion schematic



Package and pin configuration



Pin functions

pin	Pin name	Description
1	BST	Upper MOSFET Floating Bootstrap Supply. A capacitor connected between BST and SWN pins holds this bootstrap voltage for the high−side MOSFET as it is switched. The recommended capacitor value is between 100nF and 1.0μF. An external diode is required with the OC3001
2	IN	Logic−Level Input. This pin has primary control of the drive outputs
3	$\overline{OD}$	Output Disable. When low, normal operation is disabled forcing DRVH and DRVL low
4	V_{CC}	Input Supply. A 1.0 μF ceramic capacitor should be connected from this pin to PGND
5	DRVL	Output drive for the lower MOSFET
6	PGND	Power Ground. Should be closely connected to the source of the lower MOSFET
7	SWN	Switch Node. Connect to the source of the upper MOSFET
8	DRVH	Output drive for the upper MOSFET

Absolute maximum rating

symbol	description	value	unit
V_{CC}	Maximum voltage on VDD pin	18	V
V_{MAX}	Voltage range of BST/DRVH	-0.3~48	V
	Voltage range of DRVL	-0.3~VCC+0.3	
	Voltage range of SWN	-5~48	
	Voltage range of IN/$\overline{OD}$	-0.3~6.5	
R_{JA}	SOP8 thermal Resistance, Junction-to-Ambient	123	°C /W
	DFN8 thermal Resistance, Junction-to-Ambient	55	
T_A	Operation temperature range	-20~85	°C
T_{STG}	Storage temperature range	-40~150	°C
T_{SD}	Welding temp（less than 10sec.）	260	°C
V_{ESD}	ESD（HBM）	2000	V

Functional block diagram

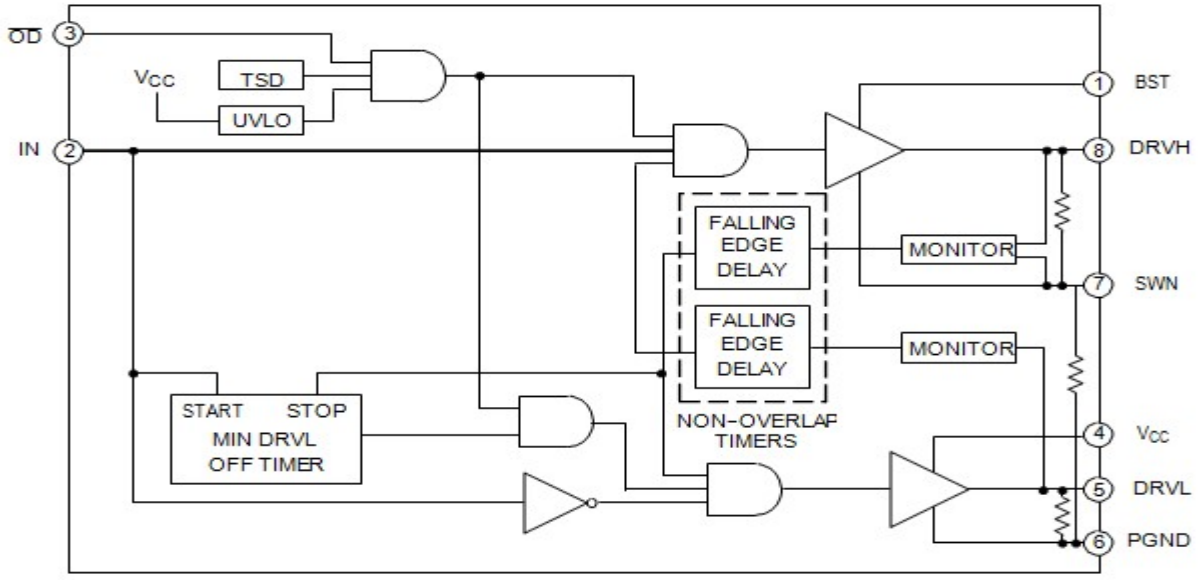


Figure1. Block Diagram

Electrical characteristics(V_{CC}=12V，T_A=0°C to 85°C, unless otherwise indicated)

Parameter	Symbol	Test Condition	Min	Typ.	Max	unit
Supply						
Supply Voltage Range	V_{CC}	-	4.6		13.2	V
Supply Current	I_{SYS}	BST=12V, IN=0V		0.7	5	mA
$\overline{OD}$ Input						
Input Voltage High	$V_{\overline{OD}\_HI}$		2			V
Input Voltage Low	$V_{\overline{OD}\_LO}$				0.8	V
Hysteresis				400		mV
Input Current		No internal pull-up or pull-down resistors	-1		1	μA
PWM Input						
Input Voltage High	V_{PWM_HI}		2			V
Input Voltage Low	V_{PWM_LO}				0.8	V
Hysteresis				400		mV
Input Current		No internal pull-up or pull-down resistors	-1		1	μA
High-Side Driver						
Output Resistance, Sourcing Current		BST-SWN=12V		2.2	3.4	Ω
Output Resistance, Sinking Current		BST-SWN=12V		1.0	1.8	Ω
Output Resistance, Unbiased		BST-SWN=0V		15		kΩ
Transition Times	t_{rDRVH} t_{fDRVH}	BST-SWN=12V, CLOAD=3.0nF (See Figure 3)		20 18	55 45	ns
Propagation Delay Times	$t_{pdhDRVH}$	BST-SWN=12V, CLOAD=3.0nF		64	100	ns

	$t_{pdlDRVH}$ $t_{pdl\overline{OD}}$ $t_{pdh\overline{OD}}$	(See Figure 3) (See Figure 2) (See Figure 2)		15 5 18	30 15 35	
SWN Pull-down Resistance		SWN to PGND		15		k Ω
Low-Side Driver						
Output Resistance, Sourcing Current				1.8	3.4	Ω
Output Resistance, Sinking Current				1.0	1.8	Ω
Output Resistance, Unbiased		V_{CC}=PGND		15		k Ω
Transition Times	t_{rDRVL} t_{fDRVL}	CLOAD=3.0nF, (See Figure 3)		18 15	50 30	ns
Propagation Delay Times	$t_{pdhDRVL}$ $t_{pdlDRVL}$ $t_{pdl\overline{OD}}$ $t_{pdh\overline{OD}}$	CLOAD=3.0nF, (See Figure 3) (See Figure 2) (See Figure 2)		59 10 10 20	100 30 35 35	ns
Timeout Delay		BST-SWN=0V		85		ns
Under voltage Lockout						
UVLO Startup			4.0	4.4	4.8	V
UVLO Shutdown			3.7	4.1	4.3	V
Hysteresis			0.1	0.3	0.5	V

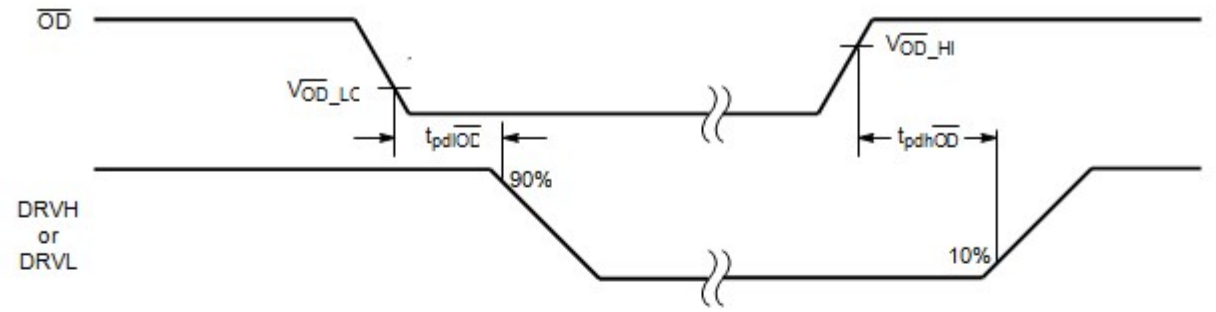


Figure 2. Output Disable Timing Diagram

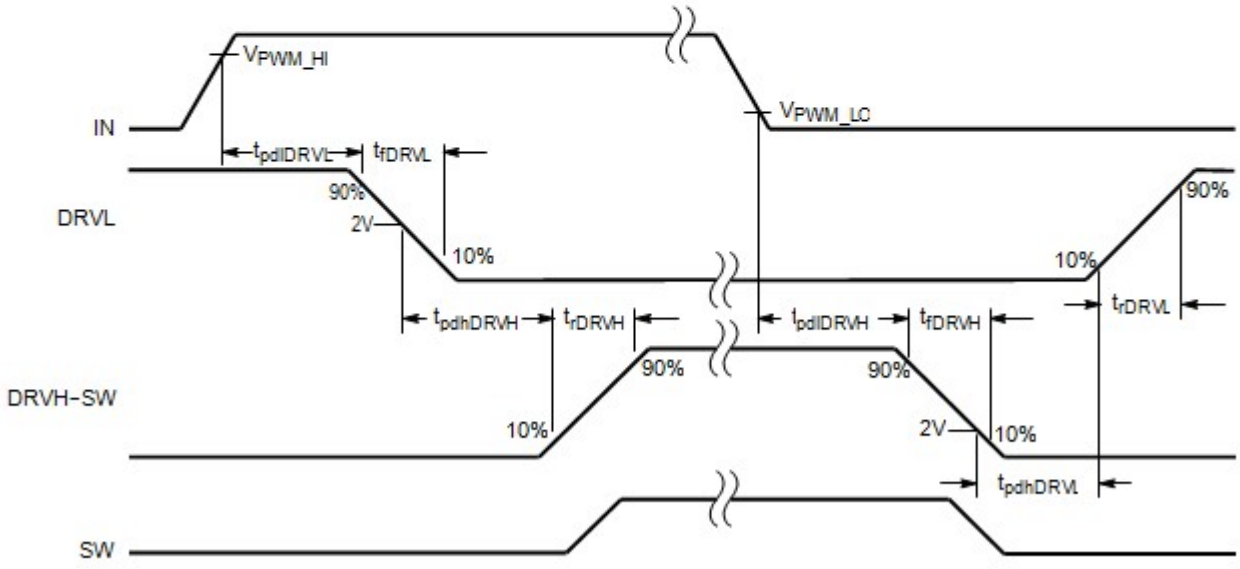


Figure 3. Nonoverlap Timing Diagram

Detail Description

Overview

The OC3001 are single phase MOSFET drivers designed for driving two N−channel MOSFETs in a synchronous buck converter topology. The OC3001 will operate from 5.0V or 12V, but have been optimized for high current multi−phase buck regulators that convert 12V rail directly to the core voltage required by complex logic chips. A single PWM input signal is all that is required to properly drive the high−side and the low−side MOSFETs. Each driver is capable of driving a 3nF load at frequencies up to 1MHz.

Low-Side Driver

The low−side driver is designed to drive a ground−referenced low $R_{DS(on)}$ N−Channel MOSFET. The voltage rail for the low−side driver is internally connected to the V_{CC} supply and PGND.

High-Side Driver

The high−side driver is designed to drive a floating low $R_{DS(on)}$ N−channel MOSFET. The gate voltage for the high side driver is developed by a bootstrap circuit referenced to Switch Node (SWN) pin.

The bootstrap circuit is comprised of an external diode, and an external bootstrap capacitor. When the OC3001 are starting up, the SWN pin is at ground, so the bootstrap capacitor will charge up to VCC through the bootstrap diode. When the PWM input goes high, the high−side driver will begin to turn on the high−side MOSFET using the stored charge of the bootstrap capacitor. As the high−side MOSFET turns on, the SWN pin will rise. When the high−side MOSFET is fully on, the switch node will be at 12V, and the BST pin will be at 12V plus the charge of the bootstrap capacitor (approaching 24 V).

The bootstrap capacitor is recharged when the switch node goes low during the next cycle.

Safety Timer and Overlap Protection Circuit

It is very important that MOSFETs in a synchronous buck regulator do not both conduct at the same time. Excessive shoot−through or cross conduction can damage the MOSFETs, and even a small amount of cross conduction will cause a decrease in the power conversion efficiency.

The OC3001 prevent cross conduction by monitoring the status of the external MOSFETs and applying the appropriate amount of “dead−time” or the time between the turn off of one MOSFET and the turn on of the other MOSFET.

When the PWM input pin goes high, DRVL will go low after a propagation delay ($t_{pdlDRVL}$). The time it takes for the low−side MOSFET to turn off (t_{fDRVL}) is dependent on the total charge on the low−side MOSFET gate. The OC3001 monitor the gate voltage of both MOSFETs and the switch node voltage to determine the conduction status of the MOSFETs. Once the low−side MOSFET is turned off an internal timer will delay ($t_{pdhDRVH}$) the turn on of the high−side MOSFET.

Likewise, when the PWM input pin goes low, DRVH will go low after the propagation delay (t_{pdDRVH}). The time to turn off the high−side MOSFET (t_{fDRVH}) is dependent on the total gate charge of the high−side MOSFET. A timer will be triggered once the high−side MOSFET has stopped conducting, to delay ($t_{pdhDRVL}$) the turn on of the low−side MOSFET

Power Supply Decoupling

The OC3001 can source and sink relatively large currents to the gate pins of the external MOSFETs. In order to maintain a constant and stable supply voltage (VCC) a low ESR capacitor should be placed near the power and ground pins. A 1μF to 4.7μF multi layer ceramic capacitor (MLCC) is usually sufficient.

Input Pins

The PWM input and the Output Disable pins of the OC3001 have internal protection for Electro Static Discharge (ESD), but in normal operation they present relatively high input impedance. If the PWM controller does not have internal pull-down resistors, they should be added externally to ensure that the driver outputs do not go high before the controller has reached its under voltage lockout threshold.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_{BST}) and the internal (or an external) diode. Selection of these components can be done after the high−side MOSFET has been chosen. The bootstrap capacitor must have a voltage rating that is able to withstand twice the maximum supply voltage. A minimum 50V rating is recommended. The capacitance is determined using the following equation:

$$C_{BST} = \frac{Q_{GATE}}{\Delta V_{BST}}$$

Where Q_{GATE} is the total gate charge of the high−side MOSFET, and ΔV_{BST} is the voltage droop allowed on the high−side MOSFET drive. For example, a NTD60N03 has a total gate charge of about 30nC. For an allowed droop of 300mV, the required bootstrap capacitance is 100nF. A good quality ceramic capacitor should be used.

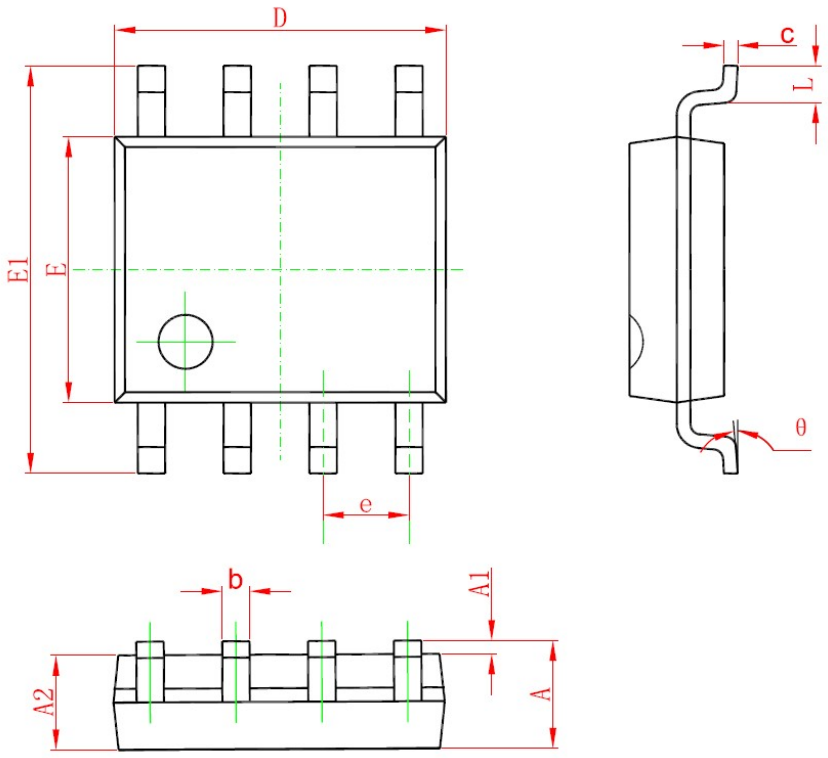
The bootstrap diode must be rated to withstand the maximum supply voltage plus any peak ringing voltages that may be present on SWN. The average forward current can be estimated by:

$$I_{F(AVG)} = Q_{GATE} \times f_{MAX}$$

where f_{MAX} is the maximum switching frequency of the controller. The peak surge current rating should be checked in−circuit, since this is dependent on the source impedance of the 12V supply and the ESR of C_{BST}.

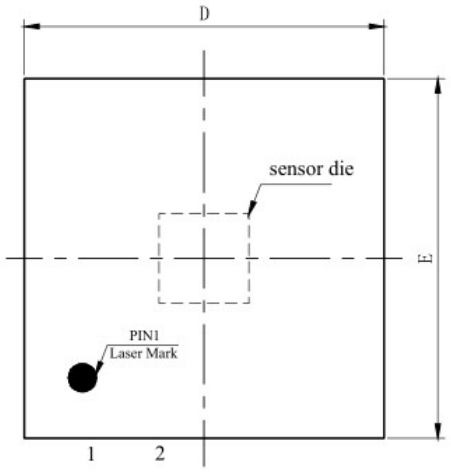
Package Information

SOP8 package outline dimensions：

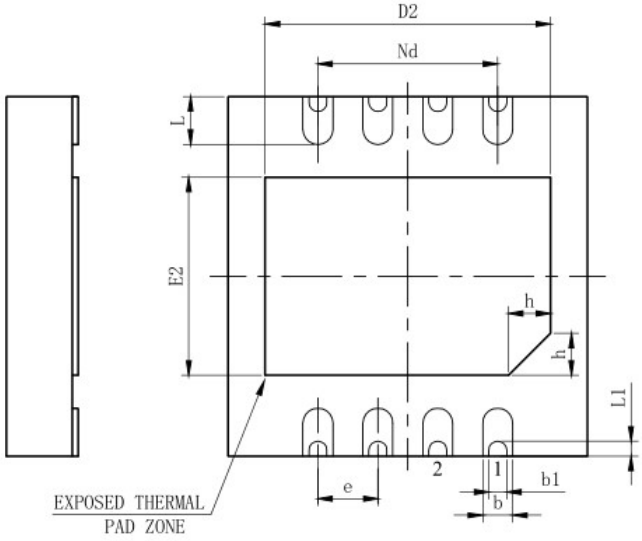


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

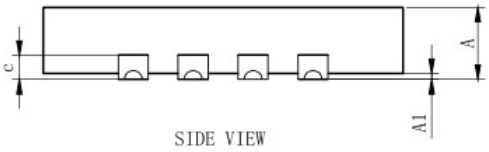
DFN8 package outline dimensions：



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.20	0.25	0.30
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	2.28	2.38	2.48
e	0.50BSC		
Nd	1.50BSC		
E	2.90	3.00	3.10
E2	1.55	1.65	1.75
L	0.30	0.40	0.50
L1	0.125REF		
h	0.30	0.35	0.40
L/F载体尺寸	2.70*1.85		